1981

ADVANCED INTERCEPTOR KA-BAND SOLID-STATE TRANSMITTER DEVELOPMENT PROGRAM

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Abstract

Requirements exist for high-power, low-noise Ka-band active interceptor seeker transmitters. This technology demonstration program has the goal of demonstrating a Ka-band solid-state transmitter with 1000 watts peak output power, 10 to 30% duty cycle, 0.05 to 50 microseconds pulse-width, 250 cu. in. of volume, and 12.5 lb in weight. These goals represent a factor of four improvement in the power density (W/cm^2) compared to the current state-of-the-art long-pulse solid-state transmitter design. To achieve these program goals, several approaches are being explored to double individual device performance and double the power-combining density of the circuits. The more successful approaches will be selected for incorporation into the final transmitter design. In the active solid-state device area, two approaches under investigation are (1) development of Indium Phosphide (InP)-based IMPATT diodes and (2) reduction of the junction to heatsink thermal resistance by using p-side carbon doping of GaAs devices. In the power-combining area, three approaches under investigation are (1) double the power density of the standard resonant module from four to eight devices by incorporating a push-pull biasing architecture or a TE_{10+} mode resonant cavity, (2) power-combining two chips per diode package, (3) power-combining several chips on waveguide-coupled planar microwave substrates.

Introduction

Operational requirements exist for intercepting and destroying hostile ballistic missiles, cruise missiles, and respective payloads in weather at low altitude. System performance tradeoff studies indicate that high-power, low-phase noise, active radar seekers operating at Ka-band (26.5 – 40 GHz) provide optimum performance.

High-power traveling wave tube (TWT)-based transmitters are the state-of-the-art for Ka-band active seekers. At present TWT-based transmitters are used in many systems. However, solid-state-based transmitters offer an alternative to the TWT-based transmitters because of the following: 1. Low FM-added noise for target detection in clutter. 2. The capability to supply low-voltage prime power directly from conventional thermal batteries, which eliminates the high-voltage switching power supply and associated issues of potential arcing and spurious switching frequency harmonic output noise. 3. Long shelf life requiring less periodic testing and requiring no outgassing. 4. Instant turn-on (no warm-up required) for fast reaction time. 5. Highly reliable, estimated 10,000 hours mean-time-to-failure when actively cooled. Passively cooled operation of 60 to 90 seconds when fired or under test. 6. Output power that degrades gracefully in the event of individual device failures so that total transmitter failure unlikely to occur.

Background

Technology development in the field of impact avalanche transit time (IMPATT) diode-based solid-state transmitters has been ongoing for several years. The state-of-the-art long-pulse (LP1) Ka-band solid-state transmitter developed by the USA/SSDC, Huntsville, Ala., in cooperation with the Naval Air Warfare Center Weapons Division, China Lake, Calif., and Raytheon Electronic Systems Division, Lexington, Mass., is shown in Figure 1. This transmitter demonstrated the performance shown in Table 1.

TABLE 1. Transmitter Performance.

Parameter	Characteristic
XMTR	LP1
Frequency	Ka-band
Bandwidth	3%
Output power	500 watts, peak
Added noise	-125 dBc/Hz at 10 kHz
Waveform	0.050 to 50 μs
Duty cycle	10% to 30%
Weight	25 lb
Volume	500 cu. in.

The LP1 program was fully successful; however, it does not meet the power, size, and weight requirements of future long-pulse interceptor systems. To meet these

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future requirements, the Advanced Interceptor Technology (AIT) program office has initiated the development of a second long-pulse (LP2) transmitter. This transmitter development effort has the program goals shown in Table 2.

TABLE 2. LP2 Program Performance Goals.

Parameter	Characteristics
XMTR	LP2
Frequency	Ka-band
Bandwidth	3%
Output power	1000 watts, peak
Added noise	-140 dBc/Hz at 10 kHz
Waveform	0.050 to 50 μs
Duty cycle	10% to 30%
Weight	12.5 lb
Volume	250 cu. in.

Comparing the LP1 and LP2 transmitters, it is seen that LP2 must be designed to have twice the output power in one-half the weight and volume of the LP1 transmitter. This technology development program explores methods to double or quadruple the power output from individual devices and explores methods to double the power-combining density of the IMPATT modules. In addition to meeting these challenging performance requirements, the transmitter cost must be affordable when procured in quantities.

Long-Pulse 2 (LP2) Transmitter Design

The LP2 transmitter design currently under consideration is shown in Figure 2, and the schematic of the injection-locked chain is shown in Figure 3. This design is similar to the previous LP1 transmitter with two main differences: (1) the main power IMPATT module is changed from a 4-diode module to an 8-diode module and, (2) each packaged active device is required to be twice as powerful as the LP1 active devices. The power-combining plate and hybrid modulator designs are expected to be similar in design to the LP1 transmitter.

The specific long-pulse Ka-band active device requirements are as follows:

Parameter	Characteristic
Device	Packaged IMPATT
Output Power	8 watts, peak
Efficiency	30%

The specific long-pulse Ka-Band IMPATT module performance required:

Parameter	Characteristic
Circuit	8-diode module
Output Power	64 watts, peak
Gain	5 dB
Volume	< 2.0 cu. in.

IMPATT Diode Development

The active microwave devices used in the transmitter are IMPATT diodes. Two approaches are being investigated to increase the output power available from these devices. One approach is to build the devices using Indium Phosphide (InP) semiconductor material. The second approach is to improve the output power of the current GaAs devices.

Indium Phosphide (InP) IMPATT Diode Development

Computer simulations conducted at China Lake of double-drift Read (DDR) IMPATT structures fabricated from InP semiconductor material have indicated that a twofold improvement in output power and DC-to-RF conversion efficiency is theoretically possible as compared to the state-of-the-art GaAs IMPATTs. Specific device performance of 8 watts output power at 30% DC-to-RF efficiency from a single long-pulse InP IMPATT device is required.

There are unique challenges involving the semiconducting material growth of IMPATT diode structures and the growth of InP semiconductor material. In addition to the InP material growth issues, the technology development is required in InP device processing, low ohmic resistance contacts and device packaging. The government, university, and industry development efforts have been initiated to address these unique technology development challenges.

Material Growth of InP Devices

InP IMPATT device development for the program is conducted under Navy/Army contract at Raytheon Electronic Systems Division. (Phase I of this three-phase program has been supported by the USA/SMDC, Huntsville, Ala.)

InP IMPATT material growth is conducted under subcontract at the University of Texas at Austin, using metal organic chemical vapor deposition (MOCVD) material growth reactor. The doping profile design specifications for the material growth are shown in Figure 4.

A capacitance-voltage measurement technique was developed to characterize the InP IMPATT wafer material. This characterization allows the wafers to be screened before any further device processing. The measured data from the new wafers are compared to theoretical plots, as shown in Figure 5, to determine whether the wafer material meets specification.

Several initial growth runs did not meet the specifications. As a result of careful analysis of the defective wafers, the source of the problem was discovered. The problem was a residual concentration of tin (Sn) (used in the reactor to grow the n-buffer layer and the n-spike). Sn remained on the wafer platter after a purge cycle and then contaminated the remaining growth cycle. The remaining Sn consequently caused non-abrupt n-side transition and p-spike compensation. This is depicted graphically in Figure 6.

This problem was solved by increasing the duration of the purge step in the InP MOCVD reactor growth runs. InP DDR wafers have now been grown that meet the design specifications. The electric field profile of one of these wafers (DD-15) is shown in Figure 7. The wafer has been qualified and submitted for further processing and DC and RF testing and evaluation.

Processing the InP Wafers

According to Raytheon materials researchers, processing of InP material into usable IMPATT mesas is more difficult compared to the GaAs material. Figure 8 shows an InP IMPATT chip with integral beam leads and heat sink.

Both boron implantation and dry-etch techniques to isolate IMPATT mesas cause surface leakage currents and "soft" reverse breakdown characteristics. The most promising technique for InP appears to be the reactive ion etching (RIE) or wet-etching technique. Chips with "hard" and also sometimes "soft" breakdowns were obtained by this approach. Various experiments with different etches (phosphoric acid, hydrochloric acid) are being conducted to realize InP IMPATT chips with no leakage currents and the required "hard" reverse voltage breakdown characteristic.

Ohmic Contact Development

The experiments to develop ohmic contact metalization techniques to ensure low-resistance contacts to InP n-type and p-type materials were conducted.

The n^+-type InP presents no problems. Using Pt-Ti-Au on n^+-InP results in the ohmic contact resistance of approximately 5×10^{-7} ohm-cm^2 at 10^{19}/cm^3 doping and 400°C. The p^+-type presents certain problems. Unacceptably high ohmic contact resistance results ($\sim 10^{-5}$ ohm-cm^2 range) when directly metallizing p^+-InP. This problem was solved by a Rh-Au to p^+ InGaAs cap layer that is grown on the p-type InP. The resultant resistance is approximately 5×10^{-7} ohm-cm^2 at 10^{19}/cm^3 doping and 400°C.

Current Status of InP Development

Several successful DDR and double-drift flat profile InP IMPATT wafers were grown, meet specifications, and are ready for processing into chips. "Wet-etch" procedures were developed for wafer characterization and wafer processing. Device packaging and the first RF testing are to be accomplished in the near future. As an alternative to Sb n-type doping, silicon (Si) n-type doping is now being investigated. Disilane gas is planned as the medium to provide the n-type Si dopant. The Si dopant should have a much smaller memory effect than the Sb. The current technical challenge using disilane gas is to control the doping level from 9×10^{15} up to 2×10^{19} cm^{-3}. One approach under investigation to control this spread is to install a second mass-flow controller for the lower doping levels of disilane. A second more readily achievable approach is the use of Sn dopant for the lightly doped levels and disilane for the highly doped levels. The memory effect is a problem only for the highly doped layers, so this should be an effective solution.

Carbon-Doped GaAs IMPATT Development

Current vapor phase epitaxy (VPE)-grown GaAs IMPATT wafers incorporate zinc (Zn) as the p-type dopant. However, recent MOCVD growth experiments at the Naval Research Laboratory using carbon-doping (C-doping) of the p-side revealed some unexpected results. These results indicated that the C-doped

IMPATTs met RF specifications and also had 20 to 30% lower thermal resistance.

The Ka-band GaAs IMPATTs are thermally limited devices. Under thermally limited operation, the available output power is inversely proportional to this thermal resistance. Therefore, a decrease in thermal resistance has the potential for increased output power from the device for a constant junction temperature rise and a constant DC-to-RF conversion efficiency. The measured decrease in the thermal resistance from 7.0°C/W to 5.14°C/W results in a potential 38% increase in the output power. This indicates that the RF power performance of GaAs IMPATTs could potentially be improved from the present 3 watts (average) to approximately 4.15 watts (average). This small increase alone could improve the current LP1 transmitter from 500 to 700 watts of output power.

This program was undertaken to understand the underlying physics behind the lower thermal resistance and then use this knowledge to improve the power and reliability of the GaAs IMPATT diodes.

Current Status of C-Doped GaAs

The heat that is dissipated in the chip flows through the p-contact, so the metal-to-semiconductor interface on this contact is critical to achieving a low thermal resistance. The reason the C-doped MOCVD wafers have lower thermal resistance may be attributable to this interface. To test this hypothesis, Sandia National Laboratories are growing additional wafers for this program with Zn as the dopant for the p-contact, which is the dopant used in the VPE reactor. Processing of both Zn-doped and C-doped wafers will be performed in the same batch to compare the thermal resistance. Currently, the C-doped wafer growth was completed and the growth for the Zn-doped wafers is being prepared. As soon as several in-specification MOCVD wafers are grown with Zn contacts, processing of these wafers along with the earlier C-doped wafers will begin so that they can be compared.

Packaged Chip-Level Power Combining

An alternative to a having a new single device that generates twice the output power is to have two of the current or improved GaAs chips power-combined inside a single package. The high level of power dissipation in each chip requires that they be mounted thermally in parallel.

Electrical analysis was performed at China Lake on several candidate chip-level package designs. Thermal analysis of these designs is planned and will be performed using finite-element analysis software.

A procedure was developed that allows the electrical characterization of chip-level power-combining package designs. The Ansoft High-Frequency (Electromagnetic) Structure Simulator (HFSS) is used in the analysis of the candidate package. Several S-parameter data files are generated using HFSS, defining the diode mesas to be metallic and dielectric for different runs. These data are then used in the EEsof Libra linear microwave circuit simulator such that an equivalent circuit design fit can be optimized. This procedure was verified by running it on the standard Ka-band package and comparing these data to the established analytical package circuit model. A drawing of the standard package and equivalent circuit model is seen in Figure 9. One electronic-parallel and two electronic-series chip-combining packages analyzed are discussed in the following paragraphs.

Parallel-Chips Package

The design and corresponding equivalent circuit is seen in Figure 10. This package is larger in diameter than the standard package to allow enough area for the two diodes to be placed side-by-side onto the gold-plated diamond heat sink. No significant difference resulted between the use of two or three bond straps.

Series Chips—Standoff Approach

The second design and equivalent circuit for series connection of the chips are seen in Figure 11. In this design the second chip is bonded onto a thin synthetic diamond standoff. This standoff isolates the chip electrically, but not thermally, and allows a series connection between the chips. Bond straps from the cathode of the second chip to the package top complete the bias circuit.

Series Chips-Package in a Package

The second and final series-connected package design is called a package in a package. This design and equivalent circuit model is seen in Figure 12. In this design there is an inner synthetic diamond package, with a gold-plated synthetic-diamond cap. The second upper diode is bonded to this cap and then connected to the top of the second outer spacer to complete the circuit. The synthetic-diamond spacer and cap are

designed to provide low thermal resistance from the upper device to the heat sink.

Electrical Comparison of Designs

The negative of the estimated terminal impedance of the standard package and the three other candidate chip-level power-combining packages is plotted over the Ka-Band in Figure 13.

The standard package is plotted for reference. This package has performed well with the current IMPATT module designs. The active terminal impedance of the standard package using long-pulse diodes is approximately -2 ohms real part and + 6 ohms reactive part at the center of the band with moderate Q over the bandwidth.

The parallel-chips package has the lowest active impedance (approximately -1 ohm) real-part impedance, but is high enough to be matched using the conventional methods. Impedance matching to lower impedance generally reduces the bandwidth of the circuit. Fortunately, however, this package has the lowest Q of the three designs, and this helps offset the bandwidth lost by matching to the lower real-part impedance.

The series-chips package designs present higher real-part terminal impedance, which is desirable for impedance matching. However, this initial analysis indicates that these designs also have higher reactance and higher Q, which makes impedance matching more difficult. Another potential concern is the slope in real-part terminal impedance versus frequency. This also adds difficulty in the impedance transformer design over the bandwidth of operation. Further optimization of these initial designs is planned to minimize the reactive swing and real-part slopes versus frequency. Comparing the two series-chips package designs, the package-in-a-package design has the preferable electrical properties. However, fabrication and thermal issues have not yet been addressed.

These initial theoretical results indicate that these chip-combining packages are feasible from an electronic standpoint. To validate these designs, further work will be performed in thermal analysis, prototype fabrication, and device test. For the series-connected pair, analysis is also required to verify that the impedance presented to each chip is the same, such as to allow each chip to generate equal and maximum output power.

IMPATT Module Development

The state-of-the-art IMPATT module used in the LP1 transmitter power combines four of the single-power IMPATT diodes. To meet the LP2 requirements, it is necessary to power-combine eight of the double-power devices in approximately the same volume (~2 cu. in., including hybrid bias modulator circuits).

Three concepts are being explored at China Lake to accomplish this task. The first approach is to modify the existing four-diode module design for push-pull biasing. The second approach is to increase the resonant cavity length to make an eight-diode TE_{104} mode resonant module. The third, highest risk and payoff approach, uses planar substrates to perform chip-level power combining and electromagnetic coupling to a TE_{101} or TE_{102} mode resonant cavity.

Eight-Diode Push-Pull TE_{102} Mode Module

The initial design attempt chosen for this objective is to use a TE_{102}-mode cavity and biasing diodes for push-pull mode of operation. The comparison between the conventional four-diode module and the new push-pull module is seen in Figure 14. The push-pull mode of operation was demonstrated in the past by a Ku-band circular cavity power oscillator with demonstrated power-combining efficiency of nearly 100% (Reference 1).

In the push-pull design, four-pairs of IMPATT diodes are placed in opposing positions on each side of the broad wall of the resonant cavity. Four inputs on the side of the module supply the IMPATTs with the DC bias modulation.

TE_{102} Push-Pull Module Symmetry

One critical aspect of resonant IMPATT module design is the electrical symmetry of the structures scattering parameter matrix. This symmetry allows each active device to operate at equal and optimum power output and is also a practical necessity for characterization and impedance matching.

Scattering-parameter symmetry analysis of the eight-diode TE_{102}-mode push-pull module design was performed. This analysis determined that this structure can be designed to have the required electrical symmetry. One key aspect of the symmetry is that it allows the initial development work of an eight-diode

module to be performed by using a two-diode push-pull structure.

Two-Diode Push-Pull IMPATT Module

As indicated previously, a working TE_{101}-mode push-pull two-diode design can be transferred to an eight-diode TE_{102}-mode design by using symmetry. Therefore, this initial research concentrated on the two-diode laboratory design shown in Figure 15. Characterization standards were developed to measure the equivalent two-port scattering parameters and cross coupling of the two-diode structure. From the scattering parameters, the oscillator efficiency and the even- and odd-mode input impedance are calculated. A linear microwave circuit simulator is then used to design the matching transformers. Figure 16 comprises plots of the odd-mode mid-cavity impedance of the module versus frequency for several different input post-gap settings. Figure 17 is a plot of the oscillator efficiency versus frequency respective of the post-gap settings. Comparing these data to a standard module, it is evident that the mid-cavity impedance at resonance is approximately one-half and the efficiency is higher for equal post-gap settings. Initially these data looked promising.

The design of the impedance-matching transformers revealed, however, that this module may not be compatible with the current method of power-amplifier impedance matching. Figure 18 contains plots of the transformed input impedance for the measured cavity and an equivalent circuit module. What is seen from the equivalent circuit model is that the out-of-band input impedance presented to the diodes contains multiple device-line/circuit line crossings. This design practice cannot be used in designing IMPATT diode circuits. Subsequent testing revealed that this module could not operate in a stable mode when presented with this impedance locus.

Past reference work demonstrated a successful push-pull IMPATT power oscillator design. The oscillator matching design of the reference was re-created for this Ka-band module and found to produce 6.2 watts output power with excellent pulse shape, 83% combining efficiency with very stable operation. This demonstrated that the devices are capable of operating in the push-pull mode. Figure 19 is a plot of the impedance matching used for the power oscillator mode. The estimated negative of the transformed device impedance is located on the right, and the quarter-wavelength transformed cavity impedance curve is on the left. On this plot it is seen that the device line and circuit line intersect at one point near the center of the Smith chart; this point is the frequency of oscillation.

To match these devices for power-added injection-locked operation requires that this negative-transformed device line impedance is moved farther to the right. This was attempted several times, but stable, power-added operation could not be obtained. This is again attributed to the loop that is generated in the impedance locus presented to the IMPATT diodes when matched in this manner.

De-Tuned Push-Pull Impedance Matching

To achieve injection-locked power-added operation from the two-diode push-pull module, a new approach was explored. In standard Kurokawa cavity designs, the impedance presented to the diodes out of the cavity resonant bandwidth is strongly influenced by the stabilization load. For the push-pull design, this is no longer the case as no current can flow into stabilization load in this mode. Characterization and analysis of this push-pull design indicated that the IMPATT diodes could be impedance matched and efficiently power combined when the cavity is off-resonance. To eliminate resonant modes, the cavity must be tuned for a fundamental-mode resonance at a frequency higher than the desired operating bandwidth.

This approach was tested and yielded the power output versus frequency shown in Figure 20. The module produced approximately 5.5 watts of added output power over a 3% bandwidth and had stable characteristics.

The de-tuned matching approach was further studied for use in power-combing four push-pull IMPATT pairs using HFSS software. This analysis indicated that operating eight devices in a de-tuned cavity mode may be possible. In this case the front and back pairs of push-pull diode sets are pushed forward, and the overall cavity length is reduced compared to a TE_{102}-mode design.

Current Status of the Push-Pull Module

Research was performed on a novel push-pull IMPATT module design. This research indicated that the push-pull approach can be used successfully in a power-oscillator mode, but the out-of-band impedance presented to the devices prohibits the use of the module

for injection-locked power-added operation when matched using the standard approach. A new impedance-matching approach was demonstrated by de-tuning the cavity to operate below the fundamental resonance. Current design efforts are underway using the HFSS software* to locate the coaxial entry line locations that allow symmetrical input impedance for an eight-diode push-pull module.

Eight-Diode TE_{104}-Mode Module

A backup approach to combining eight of the devices in a module is to use a TE_{104}-mode resonant cavity. An artist's conception of this module is seen in Figure 21. This design was considered a backup technology to the push-pull approach as the longer physical cavity length requires more volume, could possibly support additional unwanted TE waveguide modes, and has higher Q, which would reduce injection-locked bandwidth. However, this module design is an extension of the proven four-diode design. The standard four-diode module has a cavity length of one guide-wavelength. This new eight-diode module increases that length to two guide-wavelengths. This cavity length increase will increase the module size slightly over the standard four-diode module, but not to proportionally double the overall weight and volume. The volume goal for this module, including biasing modulator, is 2 cu. in. and is nearly the same as for the four-diode module.

TE_{104}-Mode 8-Diode Module Prototype

To test this module design concept, a brassboard eight-diode module was fabricated and tested. A photograph of the disassembled module is shown in Figure 22.

Broadband scattering-parameter characterization of the IMPATT module revealed that undesired modes could be excited in this cavity. These modes show up as additional peaks below and above the center frequency in the efficiency curve plotted in Figure 23. Subsequent HFSS analysis indicated that the TE_{103}- and TE_{105}-modes are responsible for the peaks.

Concern that these modes would cause problems lessened as we found that the transformed input impedance would be matched to the devices only at the center frequency. A plot of the transformed input impedance and negative of the estimated device impedance is seen in Figure 24.

Two sets of impedance transformers were fabricated and tested. The first set was designed to present a low real-part input impedance to the devices for oscillator testing. The second set presented a high real-part impedance for power-added injection-locked testing.

The pulsed-bias oscillator tests were performed over a 30-GHz bandwidth. The output spectrum of the free-running eight-diode module was compared with the noise floor of the spectrum analyzer with the module off. The comparison of these two outputs revealed that no visible spurious output is generated from the free-running eight-diode module other than the oscillation at the design frequency. This is an excellent indication that the IMPATTs have an impedance match only at the design frequency.

The injection-locked frequency-sweep output power using the second transformer set is seen in Figure 25. These data show that this first design had an output power of 31 watts. This power output is comparable to the output from two state-of-the-art four-diode modules when operated at the same pulse width and duty cycle.

Current Status of TE_{104}-Mode Module

A brassboard prototype TE_{104}-mode IMPATT module was designed and tested. The injection-locked output power obtained from the module is comparable to the output power of the two state-of-the-art four-diode modules. The injection-locked bandwidth was somewhat reduced yet acceptable for system application. No mode suppression was used in the testing. Future efforts will be to fabricate and test prototype flight-qualified production modules and perform research to increase the bandwidth and reduce the size of the modules.

Planar Cavity-Coupled IMPATT Modules

Current IMPATT transmitter design requires individually packaged active devices, machined cavities, many small parts, and labor-intensive tuning and assembly. An attractive alternative to this approach is to perform some of the IMPATT diode power-combining on planar microwave integrated circuits

* Manufactured by Ansoft.

(MIC). These planar circuits could be manufactured and tuned using automated machinery. Waveguide power-combiner plates would still be needed to efficiently power combine the individual MIC assemblies and handle the very high output-power levels.

Research was initiated to design and test planar chip-level power-combining IMPATT modules. This is a higher-risk effort compared to the other approaches discussed in this paper.

One approach that is currently being investigated is a hybrid of planar-circuit technology and the classical Kurokawa module. An artist conception of this module is shown in Figure 26. In this module stripline loops are used as a means to magnetically couple into TE_{101}-mode resonant cavity. Initial analysis of this structure using the HFSS software indicates that the efficiency and input impedance is very similar to the results obtained from conventional cavity-mode IMPATT modules. A plot of the efficiency calculated from HFSS-generated scattering parameters is shown in Figure 27, and the mid-cavity impedance is plotted in Figure 28.

The HFSS analysis indicated that this two-loop structure has excellent electrical characteristics. Consequently, it is expected that a four-loop TE_{102}-mode cavity will exhibit similar characteristics.

Critical issues associated with mounting of the IMPATT diodes are low parasitic resistance and reactance, low thermal impedance from active de ice area to heat sink, and hermetic sealing from the environment.

An initial design approach to achieve these requirements is shown in Figure 29. In this design the stripline transmission media transitions into a hermetically sealed area of microstrip transmission media. Inside the microstrip region is the IMPATT chip, thermally bonded to a diamond heat sink and electrically connected to a low-impedance transformer section. Opposite the stripline coupling-loop from the IMPATT diode is a ferrite-loaded bias feed-through and stabilization load.

It could be possible to use this structure in chip-level power combining. Figure 30 includes a series-parallel chip-level power-combining scheme similar to that demonstrated at Georgia Tech (Reference 2).

Conclusions

This program develops the technology for high-power, compact, reliable, and affordable solid-state missile seeker Ka-band transmitters for atmospheric (all-weather) interceptors.

The program objective is to develop and demonstrate a 1,000-watt peak power, high duty cycle, long-pulse seeker transmitter in 250 in^3 volume weighing less than 12.5 pounds.

The technical approaches to achieve the objectives include GaAs and InP IMPATT devices, several approaches in device power-combining techniques, and multiple-stage injection-locked transmitter architecture.

Significant progress in materials, devices, and circuits technologies has been achieved and is presented in this paper.

Growth by MOCVD reactor of the device quality multi-layered DDR InP IMPATT material meeting the design specifications in geometrical and chemical parameters has now been demonstrated.

Processing of InP IMPATT wafer material into single mesa IMPATT devices by dry and wet etching techniques has been demonstrated, resulting in IMPATT devices with sharp breakdown characteristics and low leakage.

Low-resistance ohmic contacts to p-type and n-type InP material has been developed and demonstrated.

Novel push-pull TE_{102}-mode power combining of IMPATT diodes was investigated and demonstrated. Research to gain full understanding of this high-power density (but complex) power-combining structure under injection-lock-mode continues.

Compact Kurokawa-type eight-diode TE_{104}-mode cavity power combiner was designed using HFSS electromagnetic design software, fabricated and demonstrated. The combiner performed as predicted without using mode-suppression ferromagnetic stubs in the TE_{104}-cavity walls.

Several approaches of IMPATT chip-level power combining to double the power output from a single discrete device package were analyzed. Both, series

and parallel chip combining of two chips in a single package are promising. Hardware implementation of these techniques will be accomplished in the following months.

The development of mm-wave integrated-circuit (MMIC) technology for Ka-band IMPATT power combining has been initiated. The approach has a potential for low-cost mass production of high-power and affordable missile seeker transmitters in Ka-band.

High reliability, high power in compact volume, and low FM-added noise solid-state missile seeker transmitters, being developed in this program under the sponsorship of the Atmospheric Interceptor Technology Program Office, support major defense acquisition programs for ballistic and cruise missile defense.

The seeker technology presented in this paper is being developed at the Naval Air Warfare Center Weapons Division, China Lake, Calif., in collaboration with Raytheon Electronic Systems Division.

Atmospheric Interceptor Technology Program integrators for this program are (present) Maj. John Kusnierek, U.S.A.F.; (past) Maj. Buford Shipley, U.S.A.F.

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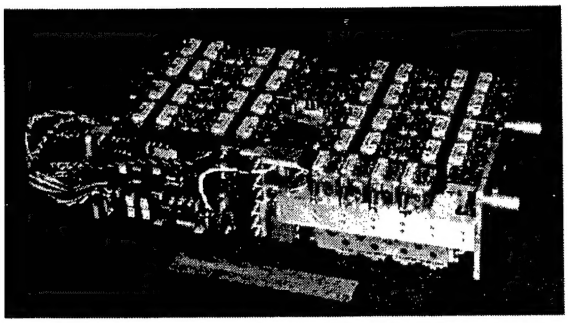


Figure 1. USA/SSDC LP1 Solid State Transmitter With Cover Removed.

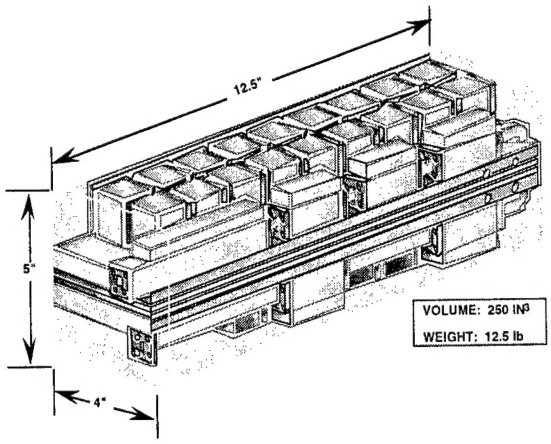


Figure 2. LP2 Transmitter Package Design.

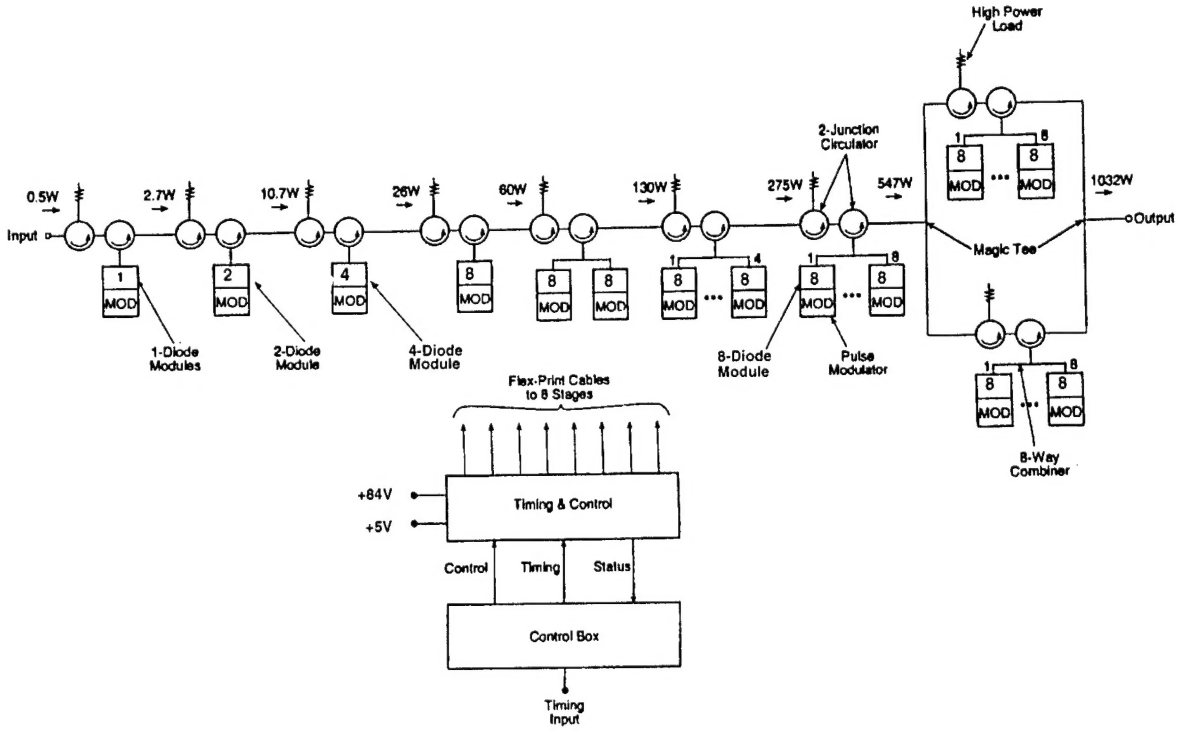


Figure 3. LP2 Injection-Lock Schematic.

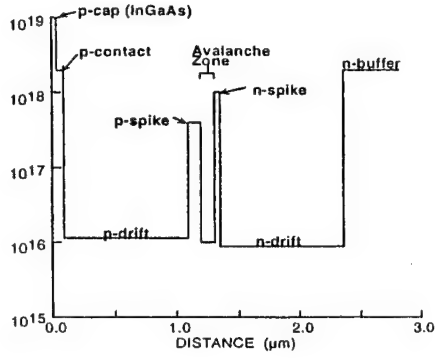


Figure 4. InP DDR IMPATT Doping Profile Specification.

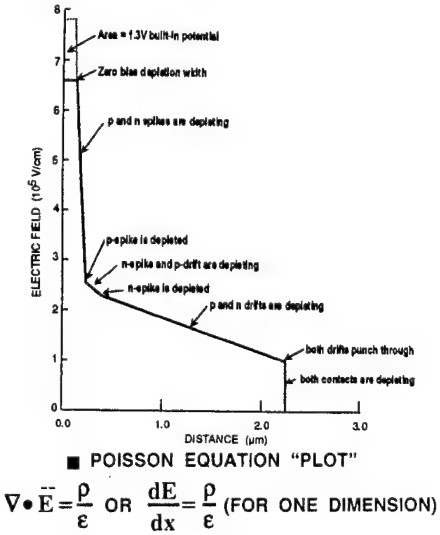


Figure 5. Electric Field Characterization Profile Plot for Double Drift Devices.

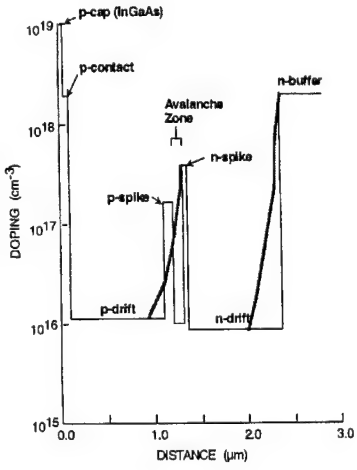


Figure 6. Memory Effect of the Tin Dopant.

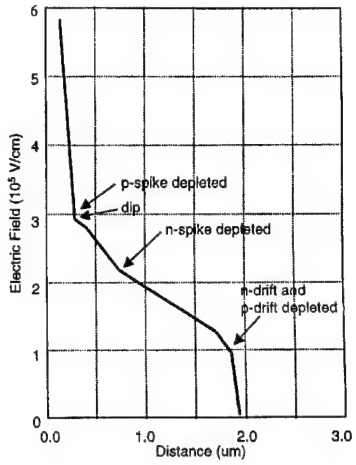


Figure 7. DD-15 Electric Field Profile.

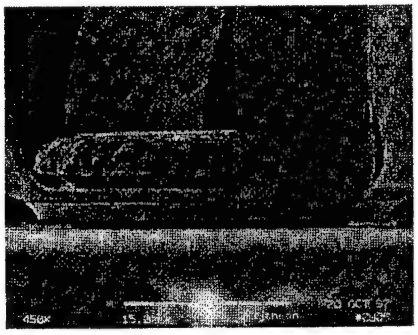


Figure 8. InP IMPATT Chip.

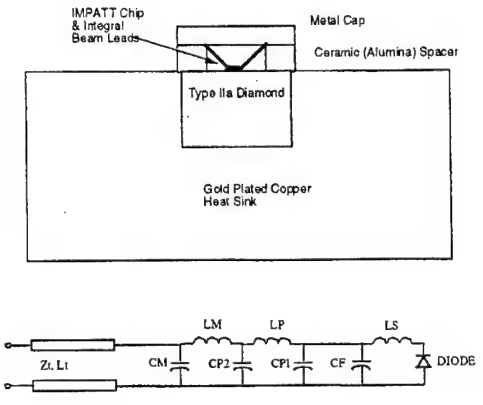


Figure 9. Standard Ka-Band Package and Lumped Element Electrical Model.

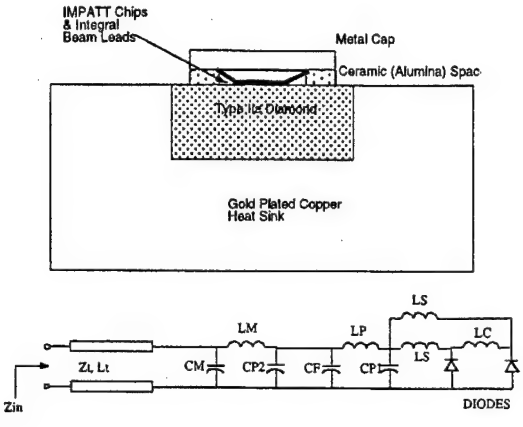


Figure 10. Parallel-Chips Package Design and Lumped Element Electrical Model.

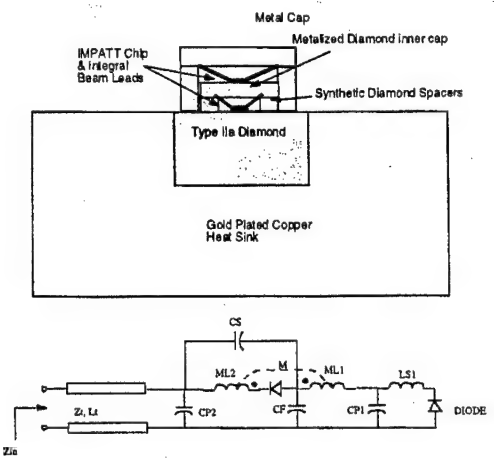


Figure 12. Series-Chips Package-in-a-Package Lumped Element Electrical Model.

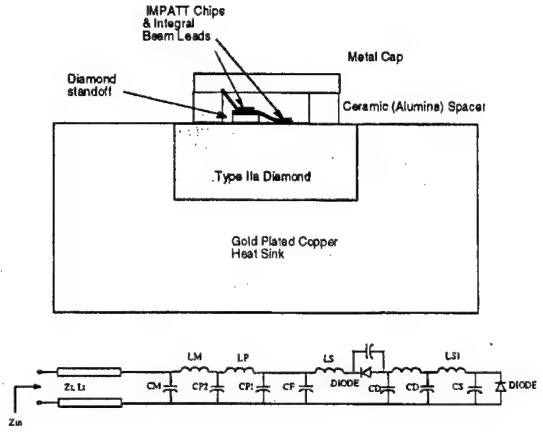


Figure 11. Series-Chips Standoff Appr ıch Package and Lumped Element Electrical Model.

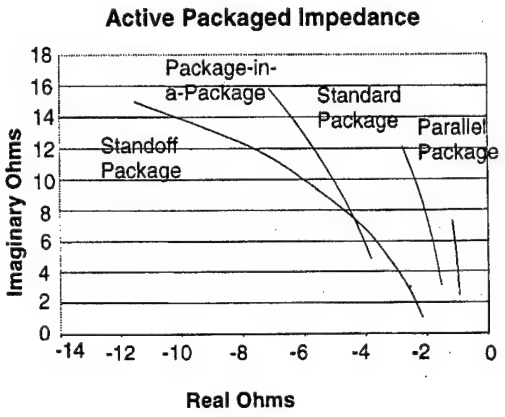
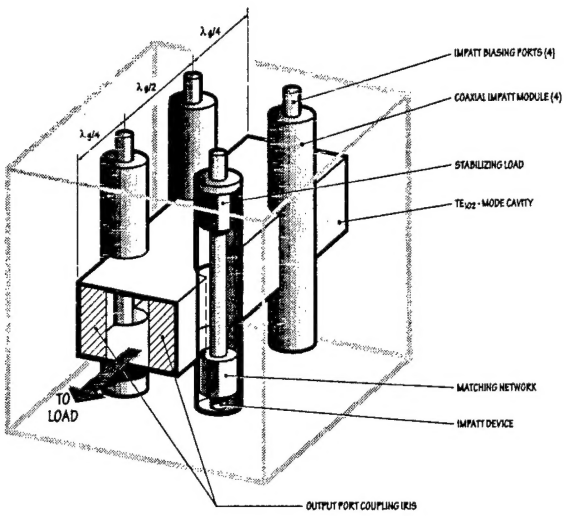
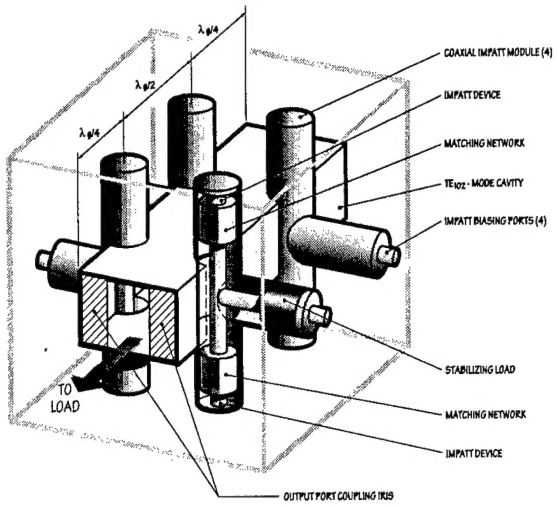


Figure 13. Estimated Active Package Impedance for Chip-Level Designs.



(a) Standard Four-Diode Module.



(b) Push-Pull Eight-Diode Module.

Figure 14. Comparison of Modules.

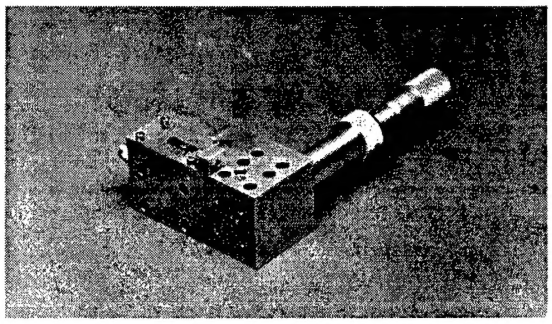


Figure 15. Laboratory TE_{101} Two-Diode Push-Pull Module.

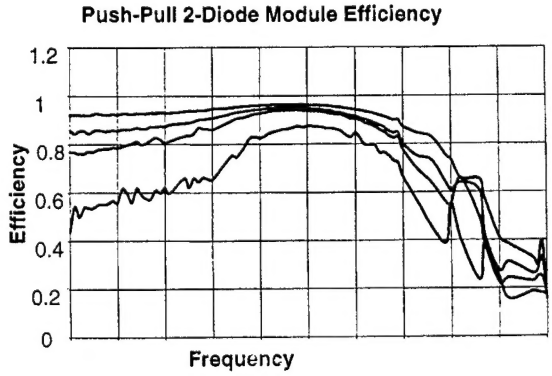


Figure 17. Two-Diode Push-Pull Module Efficiency at Four Different Post-Gap Settings.

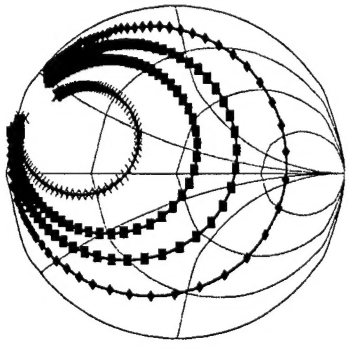
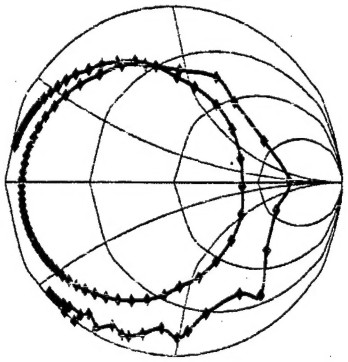
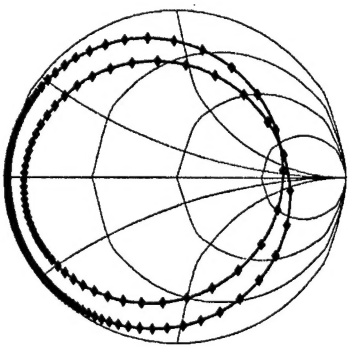


Figure 16. Two-Diode Push-Pull Odd-Mode Mid-Cavity Impedance for Four Different Post-Gap Settings.



(a) Calculated From Measured Data.



(b) Calculated Over Wider Bandwidth Using an Equivalent Circuit Model.

Figure 18. Transformed Cavity Input Impedance.

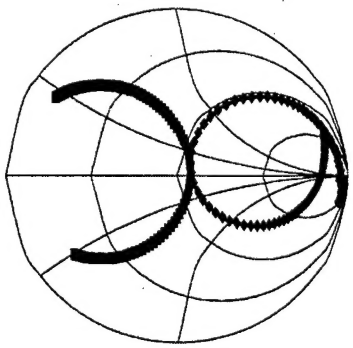


Figure 19. Power Oscillator Impedance Matching Approach.

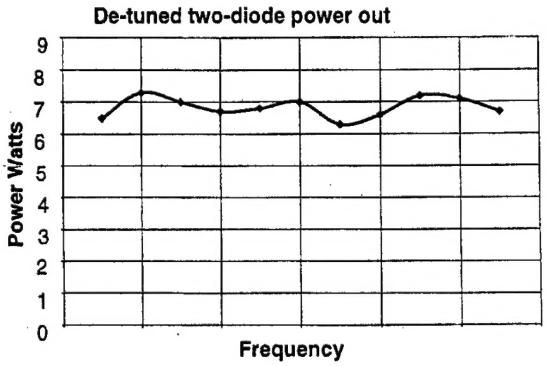


Figure 20. Frequency-Swept Power Output of Two-Diode Push-Pull Module With De-tuned Cavity Matching.

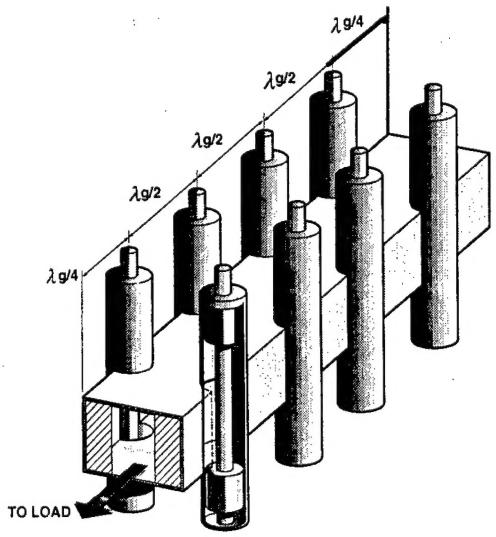


Figure 21. Eight-Diode TE_{104}-Mode Module Concept.

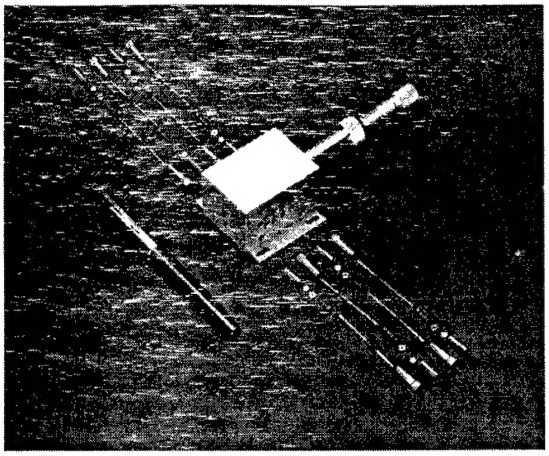


Figure 22. Laboratory Eight-Diode TE_{104}-Mode IMPATT Module Used for Testing.

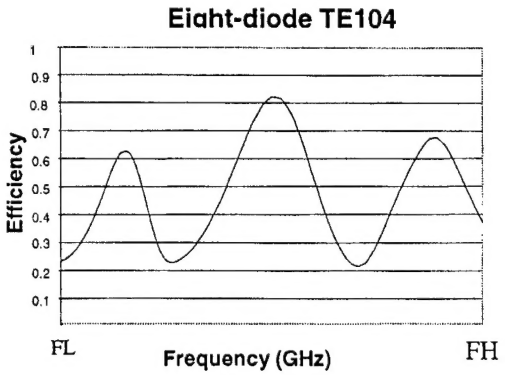


Figure 23. Eight-Diode TE_{104} Efficiency.

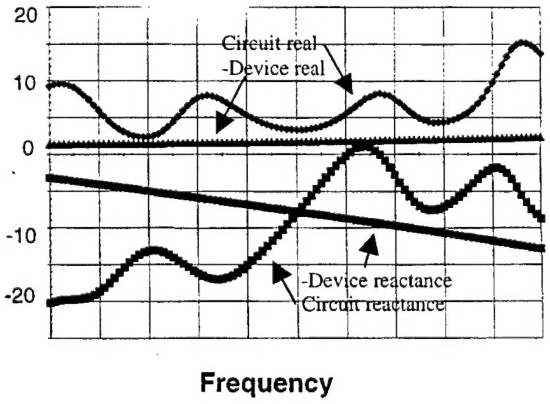


Figure 24. TE_{104}-Mode Transformed Cavity Input Impedance and Negative of the Estimated Device Impedance.

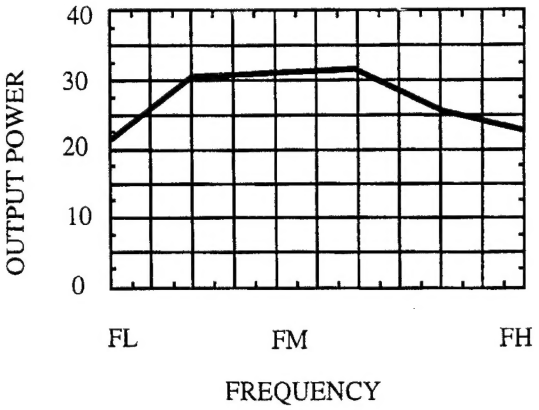


Figure 25. Power Output of Eight-Diode TE_{104}-Mode Laboratory Module.

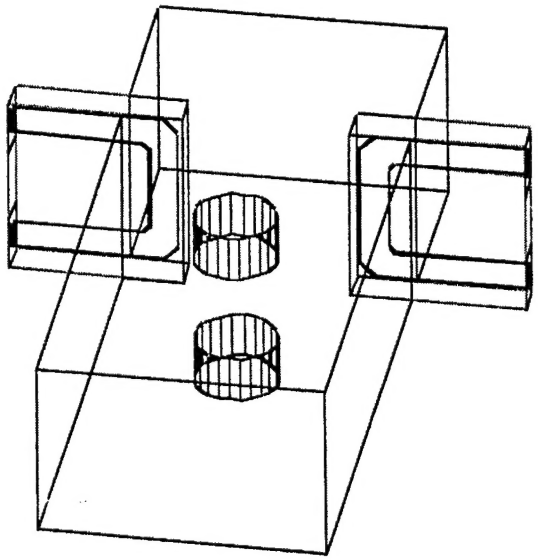


Figure 26. HFSS 3D View of Stripline Coupled Cavity.

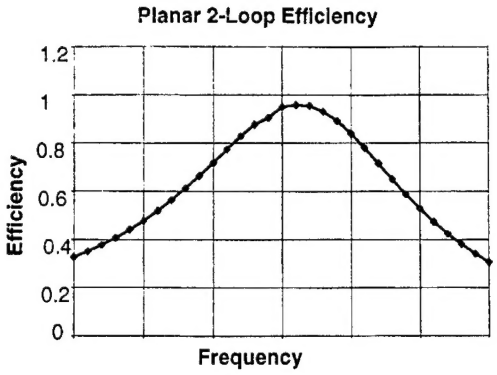


Figure 27. Planar-Coupled IMPATT Module Efficiency Calculated From HFSS s-Parameters.

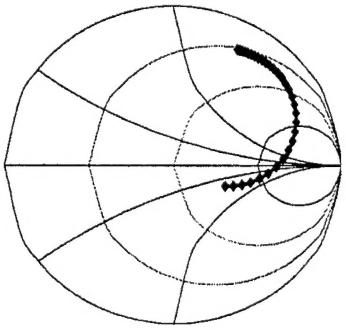


Figure 28. Planar-Coupled IMPATT Module Mid-Cavity Impedance Calculated From HFSS s-Parameters.

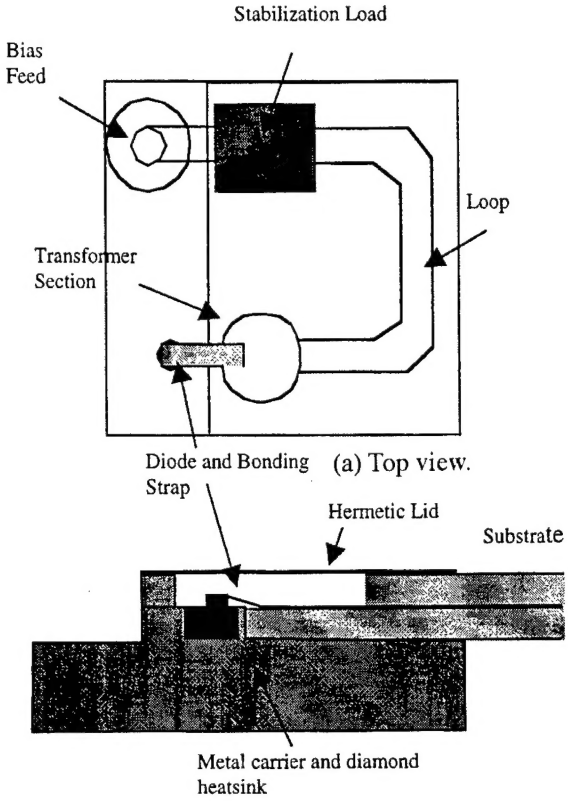


Figure 29. Planar-Coupled IMPATT Mounting Concept.

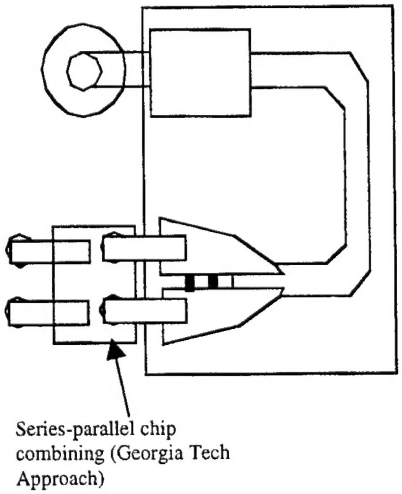


Figure 30. Chip-Level Power Combining Concept for Planar-Coupled IMPATT Mount.